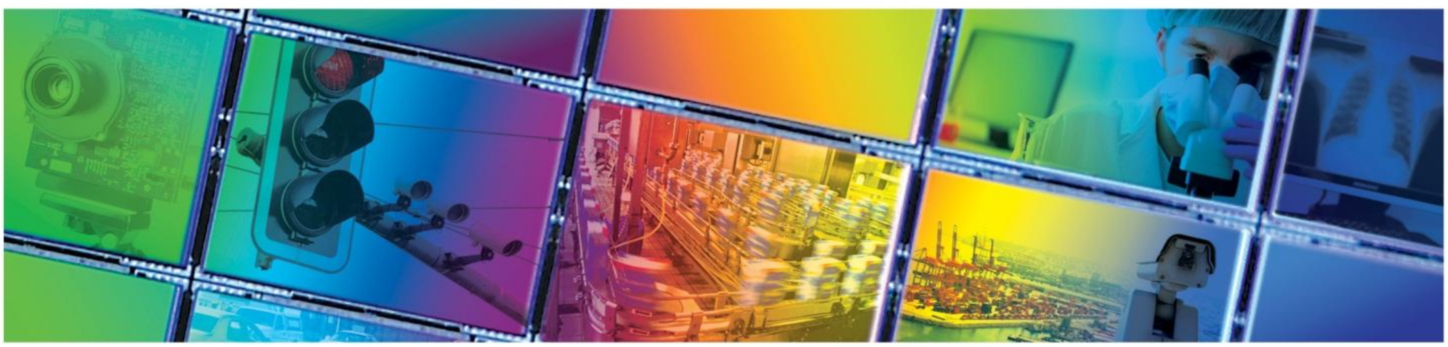
TRUESENSE imaging, inc.

KAF-0402 IMAGE SENSOR

768 (H) X 512 (V) FULL FRAME CCD IMAGE SENSOR



JULY 20, 2012

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.0 PS-0028

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Summary Specification

KAF-0402 Image Sensor

Description

The KAF-0402 Image Sensor is a high performance area CCD (charge-coupled device) image sensor with 768H x 512V photoactive pixels designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

Optional microlenses focus the majority of the light through the transparent gate, increasing the optical response further.

Applications

- Digitization
- Medical
- Scientific

Parameter	Typical Value
Architecture	Full Frame CCD; Enhanced Response
Total Number of Pixels	784 (H) x 520 (V)
Number of Active Pixels	768 (H) x 512 (V) = approx. 0.4M
Pixel Size	9.0 µm (H) x 9.0 µm (V)
Imager Size	6.91(H) mm x 4.6 (V) mm
Die Size	8.4 mm (H) x 5.5 mm (V)
Aspect Ratio	3:2
Saturation Signal	100,000 electrons
Quantum Efficiency (with microlens)	Peak: 77% 400 nm: 45%
Quantum Efficiency (no microlens)	Peak: 65% 400 nm: 30%
Output Sensitivity	10 µV/e^-
Read Noise	15 electrons
Dark Current	<10 pA/cm^2 at 25 °C
Dark Current Doubling Temperature	6.3 °C
Dynamic Range	76 dB
Charge Transfer Efficiency	>0.99999
Blooming Suppression	None
Maximum Data Rate	10 MHz
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear or AR coated, 2 sides

Parameters above are specified at 25 °C, unless otherwise noted.

Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0332	KAF- 0402-AAA-CB-B1	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Grade 1	KAF- 0402-AAA S/N
4H0334	KAF- 0402-AAA-CB-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Sample	
4H0238	KAF- 0402-AAA-CP-B1	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 1	
4H0239	KAF- 0402-AAA-CP-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
4H0240	KAF- 0402-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0234	KAF- 0402-ABA-CD-B1	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 1	KAF- 0402-ABA S/N
4H0235	KAF- 0402-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	
4H0236	KAF- 0402-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0230	KAF- 0402-ABA-CP-B1	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 1	
4H0231	KAF- 0402-ABA-CP-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
4H0232	KAF- 0402-ABA-CP-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0077	KEK-4H0077-KAF-0402-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for Truesense Imaging image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Device Description

ARCHITECTURE

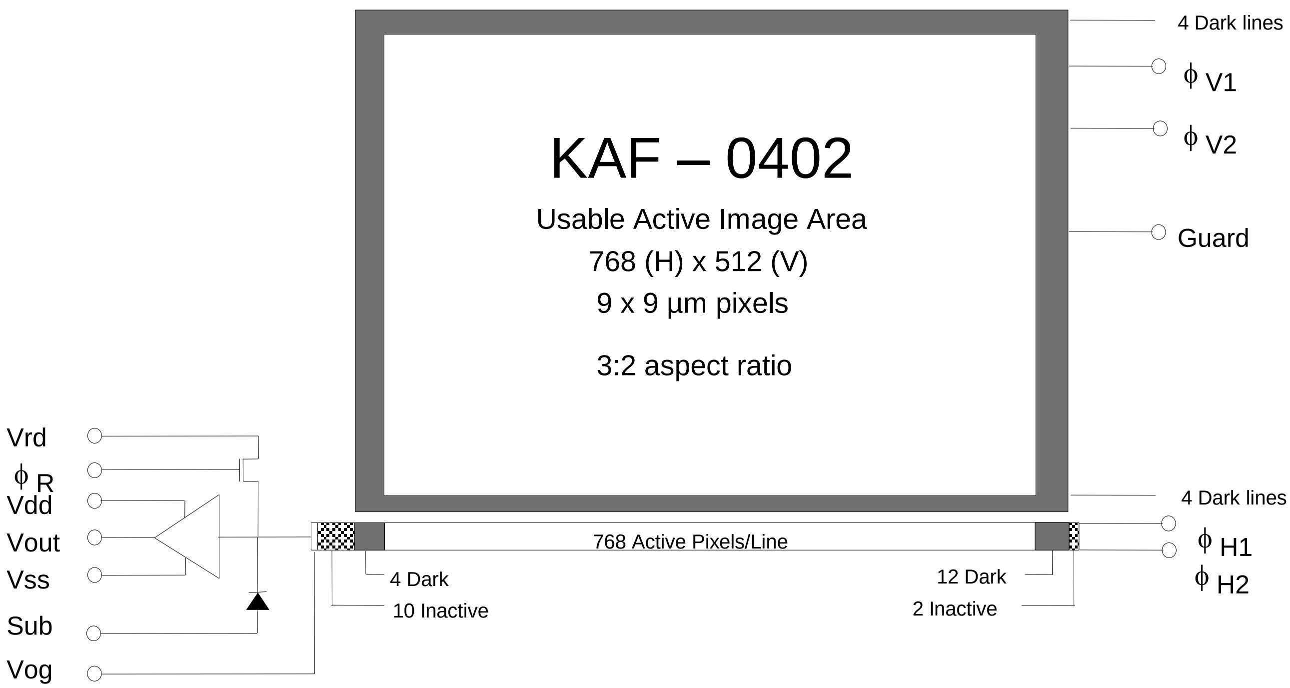


Figure 1: Block Diagram

The sensor consists of 784 parallel (vertical) CCD shift registers each 520 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 796-element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

MICROLENSES

Microlenses are formed along each row. They are effectively half of a cylinder centered on the transparent gates, extending continuously in the row direction. They act to direct the photons away from the polysilicon gate and through the transparent gate. This increases the response, especially at the shorter wavelengths (< 600 nm).

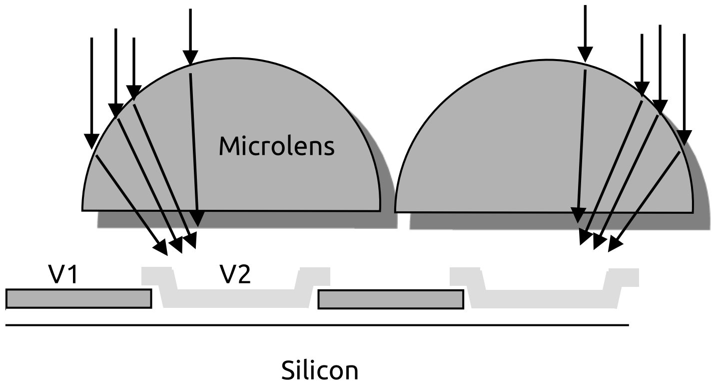


Figure 2: Microlens

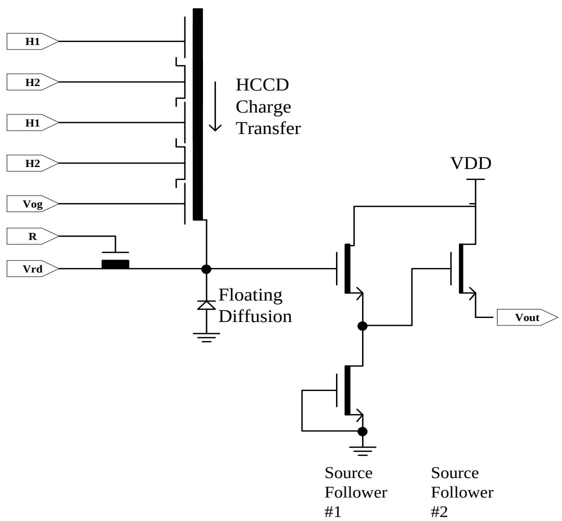


Figure 3: Output Schematic

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the floating diffusion is reset to the potential applied by Vrd (see Figure 3). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device such as shown in Figure 4.

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line, and 12 at the end. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 10 leading additional pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 9.

Charge Transport

Referring again to Figure 9, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Physical Description

Pin Description and Device Orientation

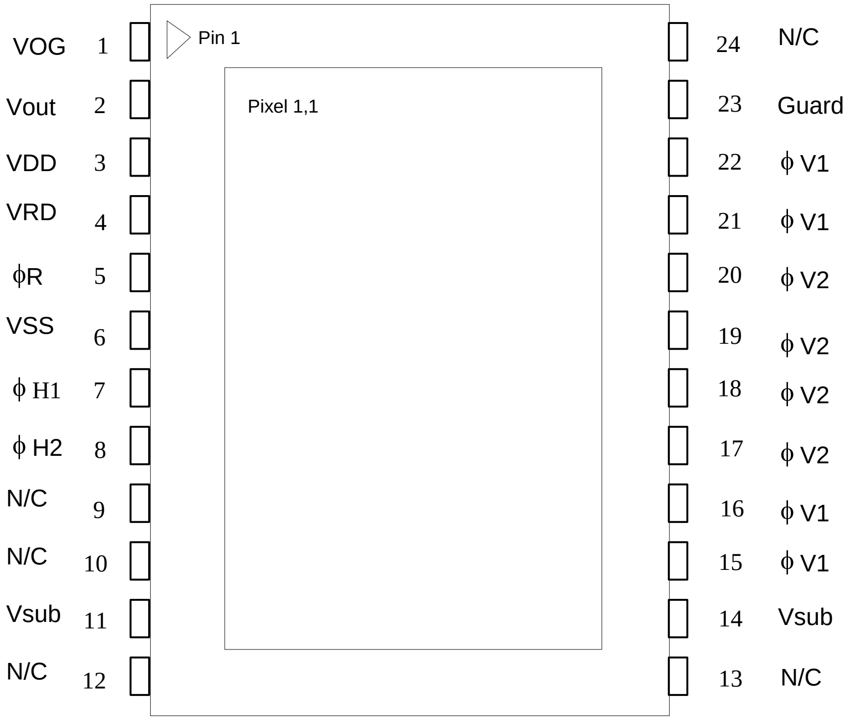


Figure 4: Pinout Diagram

Pin	Name	Description
1	OG	Output Gate
2	VOUT	Video Output
3	VDD	Amplifier Supply
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Amplifier Supply Return
7	ϕH1	Horizontal CCD Clock - Phase 1
8	ϕH2	Horizontal CCD Clock - Phase 2
9	N/C	No Connection
10	N/C	No Connection
11	VSUB	Substrate
12	N/C	No Connection

Pin	Name	Description
24	N/C	No Connection
23	GUARD	Guard Ring
22	ϕV1	Vertical CCD Clock - Phase 1
21	ϕV1	Vertical CCD Clock - Phase 1
20	ϕV2	Vertical CCD Clock - Phase 2
19	ϕV2	Vertical CCD Clock - Phase 2
18	ϕV2	Vertical CCD Clock - Phase 2
17	ϕV2	Vertical CCD Clock - Phase 2
16	ϕV1	Vertical CCD Clock - Phase 1
15	ϕV1	Vertical CCD Clock - Phase 1
14	VSUB	Substrate
13	N/C	No Connection

Imaging Performance

SPECIFICATIONS

Electro-Optical

All values measured at 25 °C and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	85000 170000 190000	100000 200000 220000	240000	electrons/pixel	1	design[9]
Quantum Efficiency (see Figure 5)							design[9]
Photoresponse Non-Linearity	PRNL		1.0	2.0	%	2	
Photoresponse Non-Uniformity	PRNU		0.8		%	3	die[8]
Dark Signal	Jdark		15 6	30 10	electrons/pixel/sec pA/cm^2	4	die[8]
Dark Signal Doubling Temperature			6.3	7	°C		design[9]
Dark Signal Non-Uniformity	DSNU		15	30	electrons/pixel/sec	5	die[8]
Dynamic Range	DR	72	76		dB	6	design[9]
Charge Transfer Efficiency	CTE	0.99997	0.99999				die[8]
Output Amplifier DC Offset	Vodc	Vrd	Vrd + 0.5	Vrd + 1.0	V		design[9]
Output Amplifier Sensitivity	$Vout/Ne^-$	9	10		$\mu V/e^-$		design[9]
Output Amplifier Output Impedance	Zout	180	200	220	Ohms		design[9]
Noise Floor	ne^-		15	20	electrons	7	

Notes:

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs.
2. Worst case deviation from straight line fit, between 2% and 90% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly at half of saturation.
4. Average of all pixels with no illumination at 25 °C.
5. Average dark signal of any of 11 x 8 blocks within the sensor (each block is 128 x 128 pixels).
6. 20log ($Nsat/ne^-$) at nominal operating frequency and 25 °C.
7. Noise floor is specified at the nominal pixel frequency and excludes any dark or pattern noises. It is dominated by the output amplifier power spectrum with a bandwidth = 5 * pixel rate.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.

Typical Performance Curves

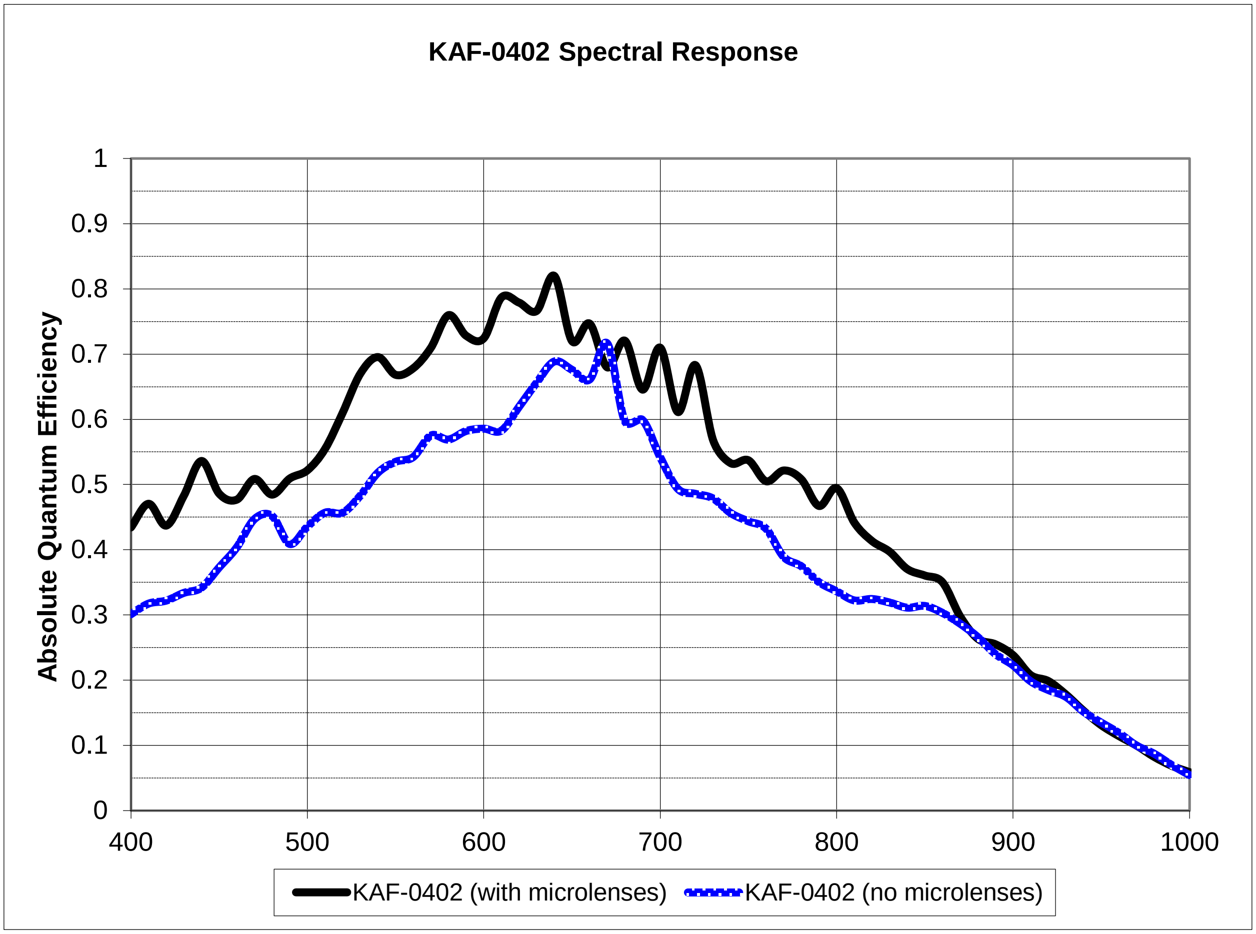


Figure 5: Typical Spectral Response

Defect Definitions

Specifications

Defect tests performed at T = 25 °C.

Grade	Point Defect	Cluster Defect	Column Defect
C1	<5	0	0
C2	<10	<4	0

Dark Defects A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

Bright Defect A pixel whose dark current >5000 electrons/pixel/second at 25 °C

Cluster Defect A grouping of not more than 5 adjacent point defects

Column Defect A grouping of >5 contiguous point defects along a single column

A column containing a pixel with dark current >12,000 electrons/pixel/second at 25 °C (Bright Column)

A column that does not meet the minimum vertical CCD charge capacity (Low charge capacity column)

A column that loses >250 electrons under 2 Ke- (trap defect)

Neighboring Pixels The surrounding 128 x 128 pixels of ± 64 columns/rows

Defect Separation Column and cluster defects are separated by no less than 2 pixels in any direction (excluding single pixel defects.

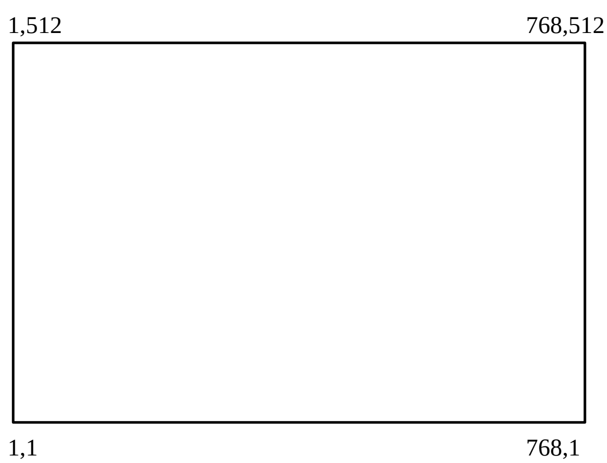


Figure 6: Active Pixel Region

Operation

Absolute Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages	Vgate1	-16	16	V	1,3,5
Output Bias Current	Iout		-10	mA	4
Output Load Capacitance	Cload		15	pF	4

Notes:

1. Referenced to pin Vsub or between each pin in this group.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2, Vog, Vlg. ϕR.
4. Avoid shorting output pins to ground or any low impedance source during operation.
5. This sensor contains gate protection circuits to provide some protection against ESD events. The circuits will turn on when greater than 16 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

Warning:

This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note *Image Sensor Handling and Best Practices.*

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd	10	11.0	11.5	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	Vdd	14.75	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	3.75	4	5	V	0.01	
Guard Ring	Vlg	8.0	9.0	12.0	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure 7 below.

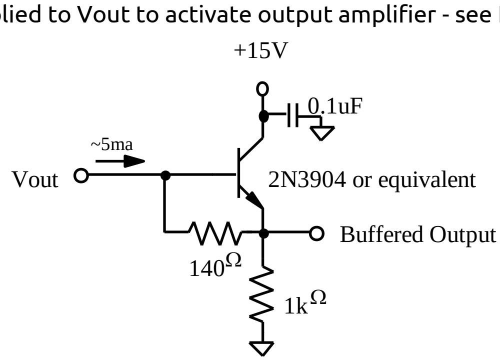


Figure 7: Example Output Structure Load Diagram

AC Operating Conditions

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	ϕV1	Low	-10.5	-10.0	-9.5	V	6 nF (all ØV1 pins)
Vertical CCD Clock - Phase 1	ϕV1	High	-0.5	0	1.0	V	6 nF (all ØV1 pins)
Vertical CCD Clock - Phase 2	ϕV2	Low	-10.5	-10.0	-9.5	V	6 nF (all ØV1 pins)
Vertical CCD Clock - Phase 2	ϕV2	High	-0.5	0	1.0	V	6 nF (all ØV1 pins)
Horizontal CCD Clock - Phase 1	ϕH1	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock - Phase 1	ϕH1	Amplitude	9.5	10.0	10.5	V	50 pF
Horizontal CCD Clock - Phase 2	ϕH2	Low	-4.5	-4.0	-3.5	V	50 pF
Horizontal CCD Clock - Phase 2	ϕH2	Amplitude	9.5	10.0	10.5	V	50 pF
Reset Clock	ϕR	Low	-3.0	-2.0	-1.75	V	5 pF
Reset Clock	ϕR	Amplitude	5.0	6.0	7.0	V	5 pF

Notes:

1. All pins draw less than 10 μA DC current.
2. Capacitance values relative to VSUB.

Timing

Requirements and Characteristics

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		4	10	MHz	1, 2, 3
Pixel Period (1 Count)	t_{pix}	100	250		ns	
ϕH1, ϕH2 Set-up Time	$t_{\phi HS}$	0.5	1		µs	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	1.5	2		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	43.7	107		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	84.1	206		µs	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (520 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (796 * t_e) + t_e$

Frame Timing

Frame Timing

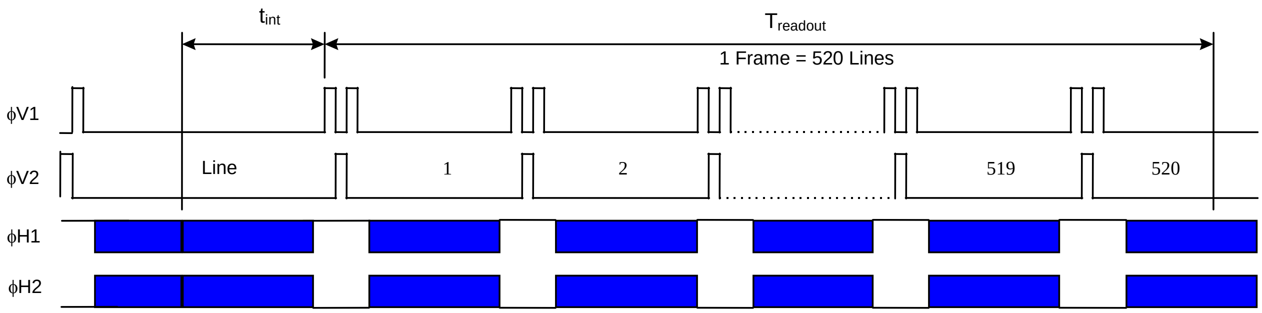
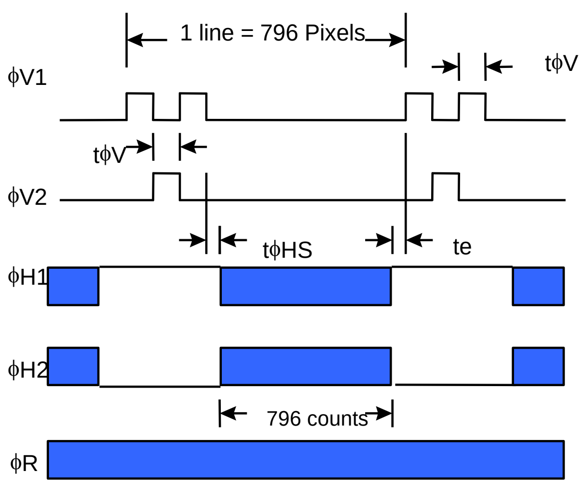


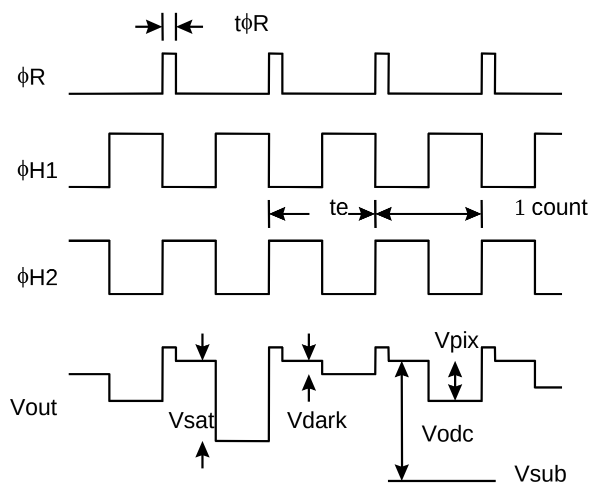
Figure 8: Frame Timing Diagram

Line Timing and Pixel Timing

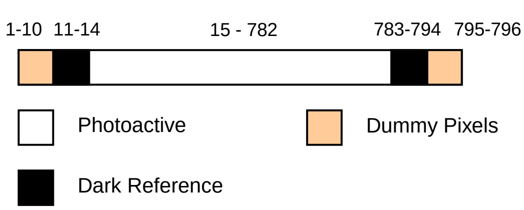
Line Timing



Pixel Timing



Line Content



Vsat	Saturated pixel video output
Vdark	Video output signal in no light situation, not zero due to
Vpix	Pixel video output signal level, more electrons =more
Vodc	Video level offset with respect to
Vsub	Analog

* See Image Aquisition section

Figure 9: Line and Pixel Timing Diagrams

Storage and Handling

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}		100	°C	
Humidity	RH	5	90	%	1

Notes:
1. T = 25 °C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

Cover Glass Care and Cleanliness

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices.*

Environmental Exposure

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions.*
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.

Mechanical Information

Completed Assembly

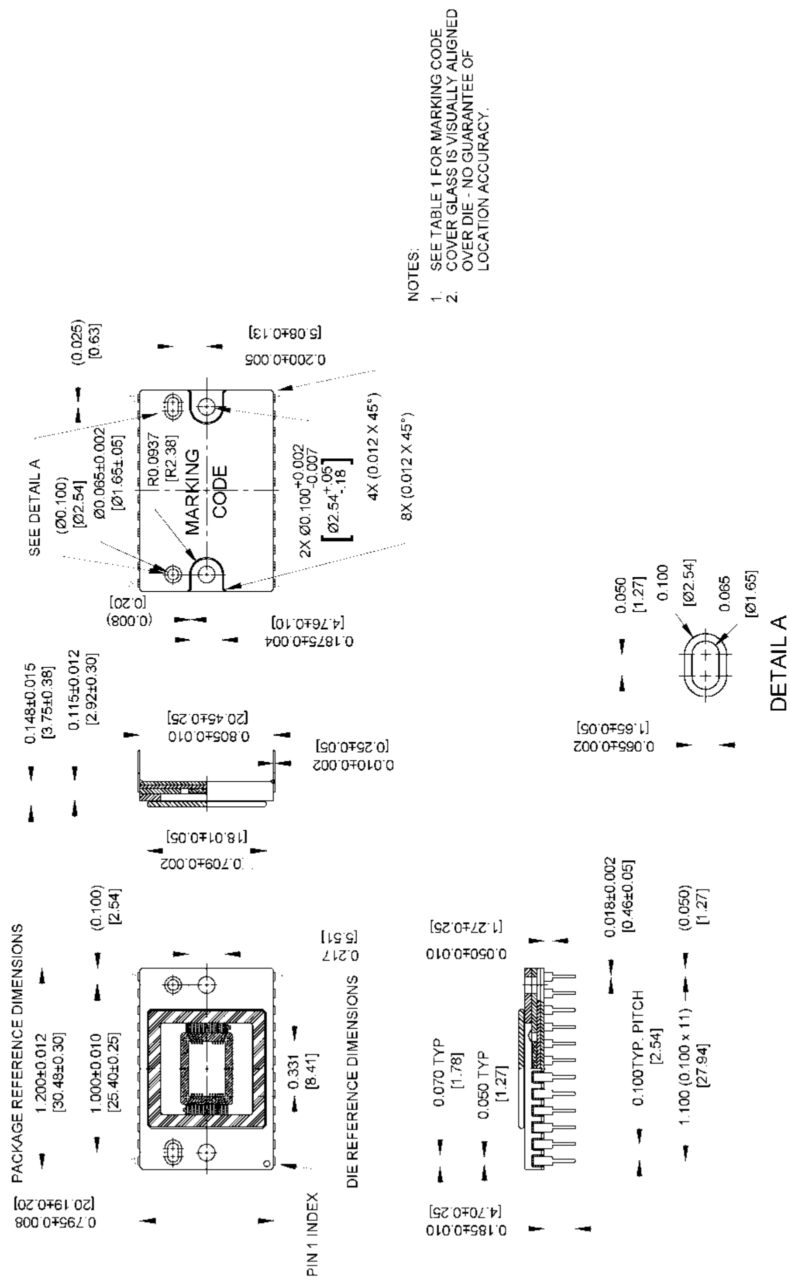


Figure 10: Completed Assembly (1 of 2)

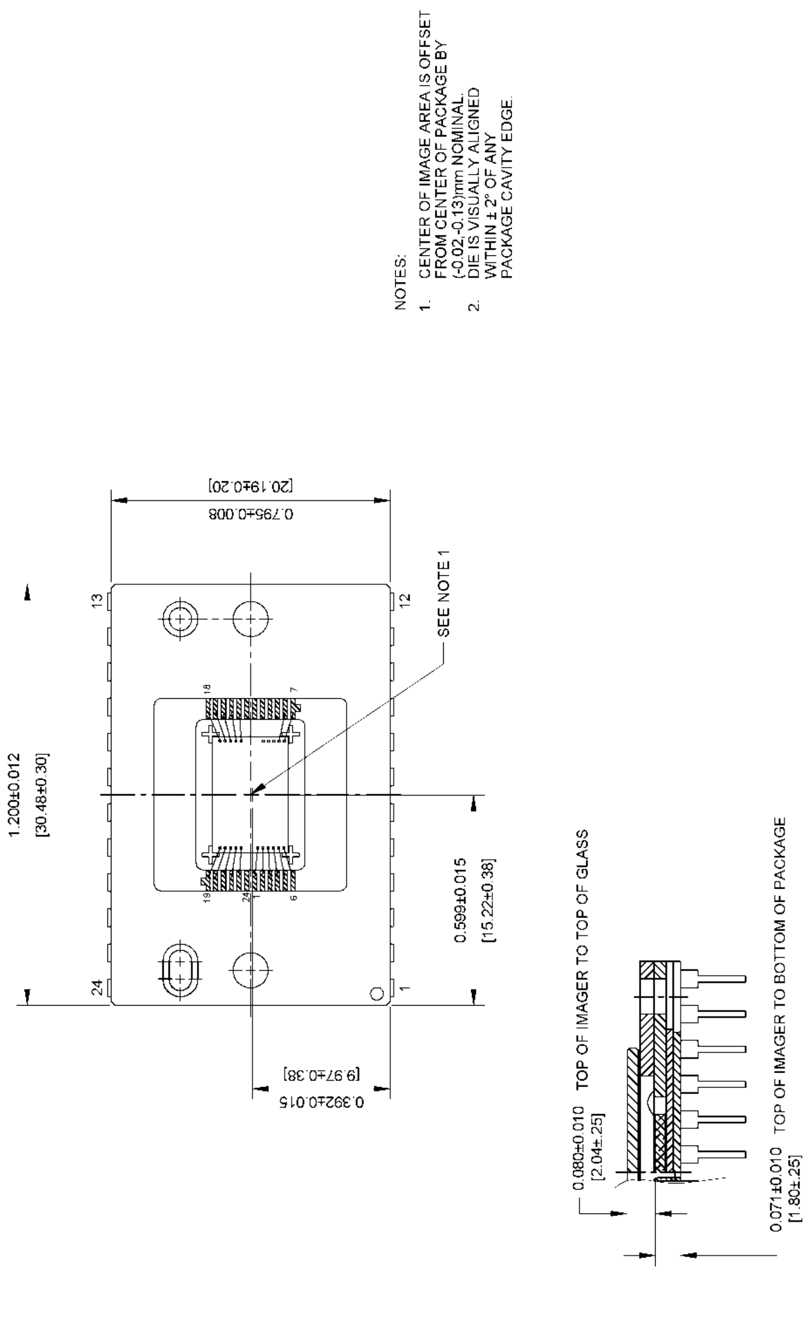


Figure 11: Completed Assembly (2 of 2)

Quality Assurance and Reliability

Quality and Reliability

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from Truesense Imaging upon request. For further information refer to Application Note *Quality and Reliability*.

Replacement

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

Liability of the Supplier

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

Liability of the Customer

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Test Data Retention

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical

The device assembly drawing is provided as a reference.

Truesense Imaging reserves the right to change any information contained herein without notice. All information furnished by Truesense Imaging is believed to be accurate.

Life Support Applications Policy

Truesense Imaging image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of Truesense Imaging, Inc.

Revision Changes

MTD/PS-0509

Revision Number	Description of Changes
1.0	• Corrected Figure 4 • Updated DC Operating Conditions, Section 2.4. • Updated CCD Parameters Specific to Low Gain (high dynamic range) Output Amplifier (page 13)
2.0	• Corrected Figure 4. (Pixel locations incorrect.) • Updated DC Operating Conditions for Output Gate (Section 2.4). • Updated CCD parameters Specific to Low Gain (High Dynamic Range) Output Amplifier for Dynamic Range (page 13). • Removed appendix.
3.0	• First version of the document in S9K. Formerly Revision 2 in hard copy format. • Removed Class 0 from the Cosmetic Specification and UV coated device. (Section 3.2) • Added ESD classification. (Section 2.3) • Replaced Quality and Reliability notes with current format. (Section 4.2)
4.0	• Update specification format • Updated Completed Assembly Drawing
5.0	• Removed 4H0333

PS-0028

Revision Number	Description of Changes
1.0	• Initial release with new document number, updated branding and document template • Updated *Storage and Handling* and *Quality Assurance and Reliability* sections